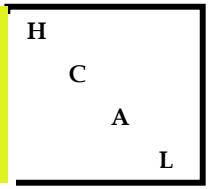
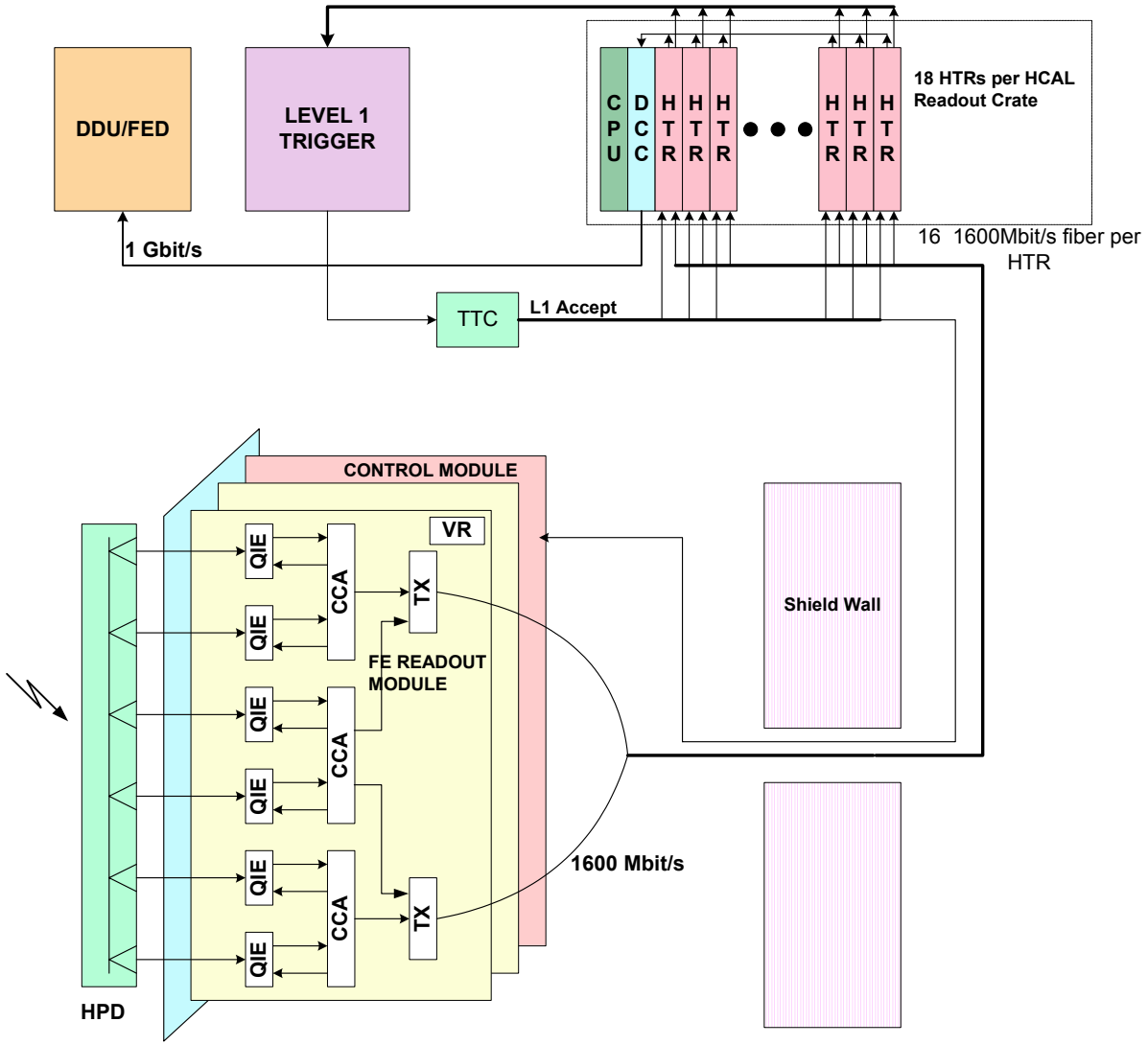
HCAL Front End Electronics



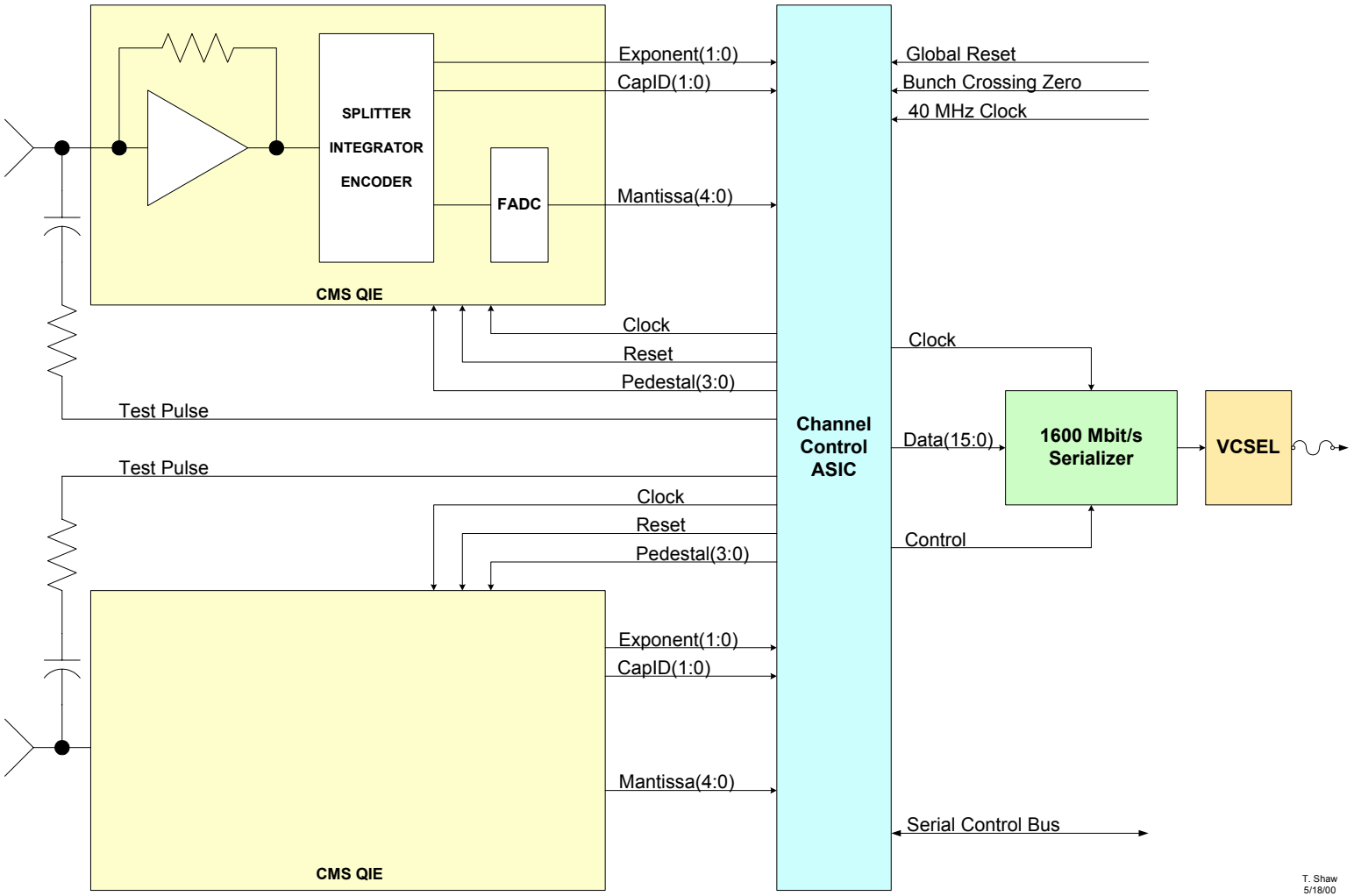
CMS Week

December, 2001

FE/DAQ Readout



FE Channels



CMS QIE Solution

FE Status

Past 6 months

- Tested proto CCA Asic – looks good
- Tested proto QIE Asic
  - Does not run at 40MHz (easy fix)
  - Noise levels under study
    - 4000e- rms with soldered coax connections btw HPD and QIE
- HB Backplane layout complete
- Proto GOL (serializer) tested - OK
  - Gigabit Ethernet protocol
  - 1600 Mbits/s
- Proto VCSEL and custom package tested – ok
- Rad qualified “glue” logic parts

QIE Description

QIE

Charge Integrator Encoder

4 stage pipelined device (25ns per stage)

- charge collection
- settling
- readout
- reset

Inverting (HPDs) and Non-inverting (PMTs) Inputs

Internal non-linear Flash ADC

Outputs

- 5 bit mantissa
- 2 bit range exponent
- 2 bit Cap ID

QIE Specification

QIE Design Specifications

- Clock > 40 MHz
- Must have inverting and non-inverting inputs
- Charge sensitivity of lowest range – 1fC/LSB
  - In Calibration Mode 1/3 fC/LSB
- Maximum Charge – 9670 fC/25ns
- 4500 electrons rms noise
- FADC Differential Non-Linearity < .05 LSBs

CMS QIE Status

Full chip submitted 3/13/01

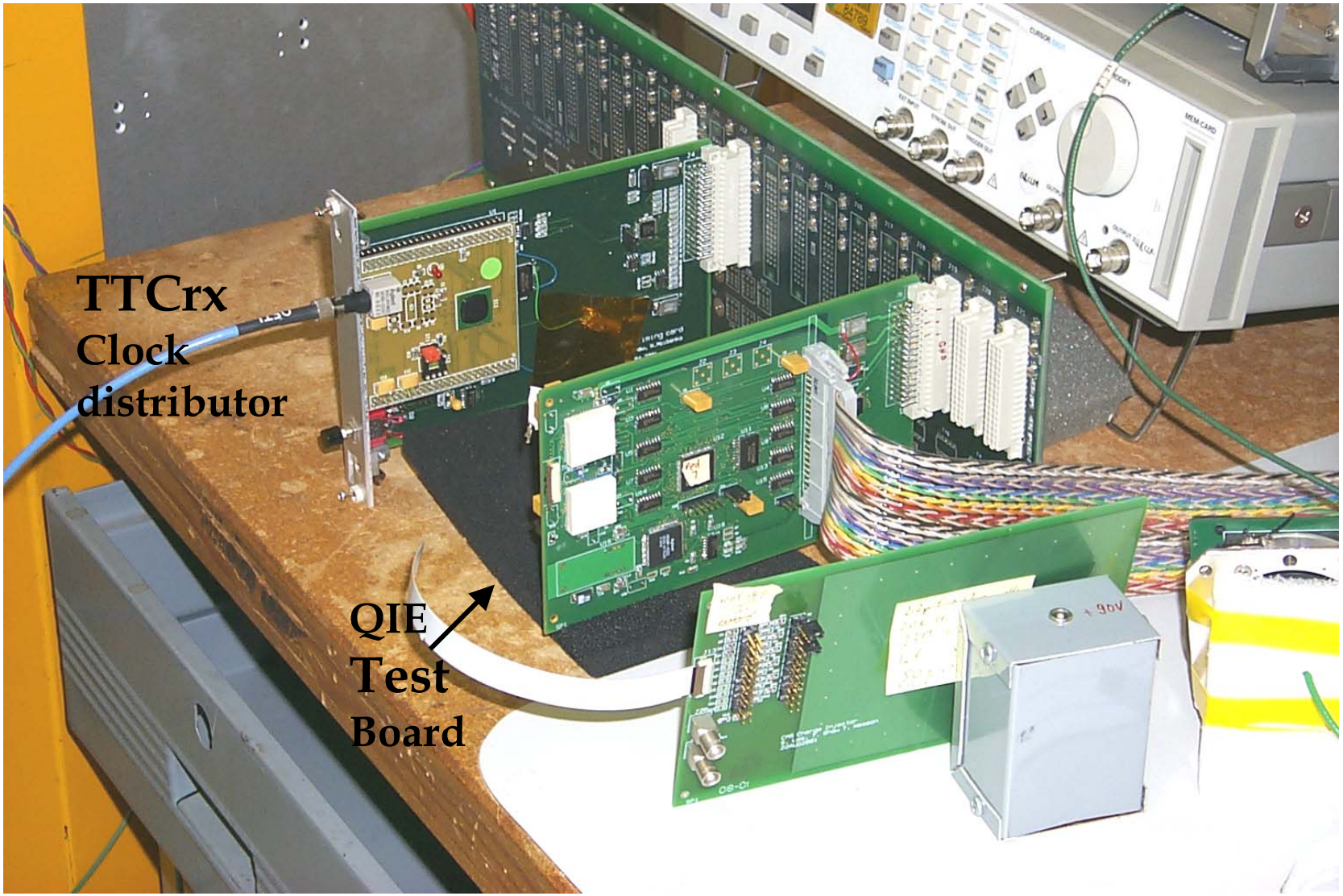
Received 5 wafers 6/1/01

Testing shows chip fully functional

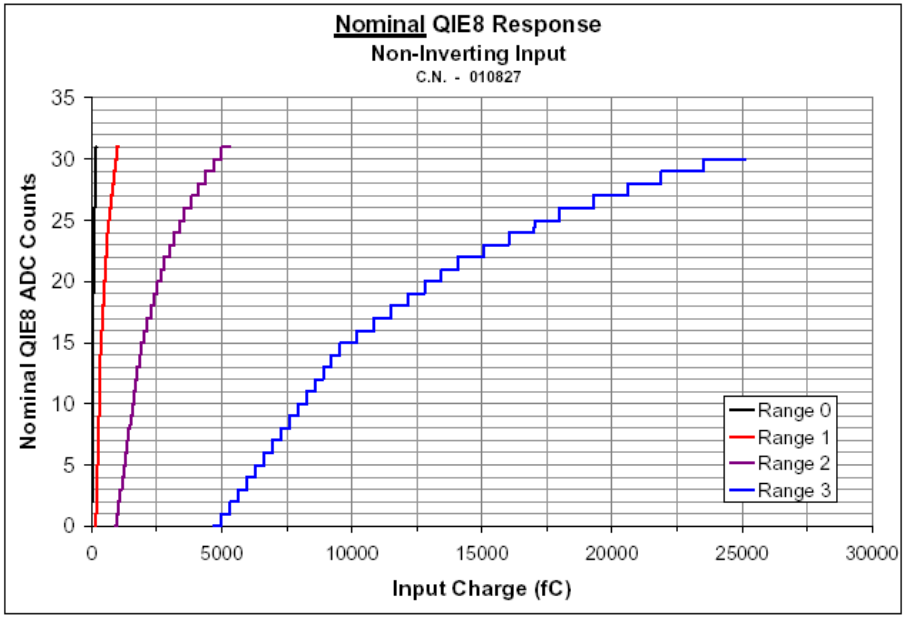
- **Chip does not run at 40 MHz**
- **Noise as a function of input capacitance being studied**
- **Noise of 4000e- rms achieved with soldered coax connections btw HPD and QIE**

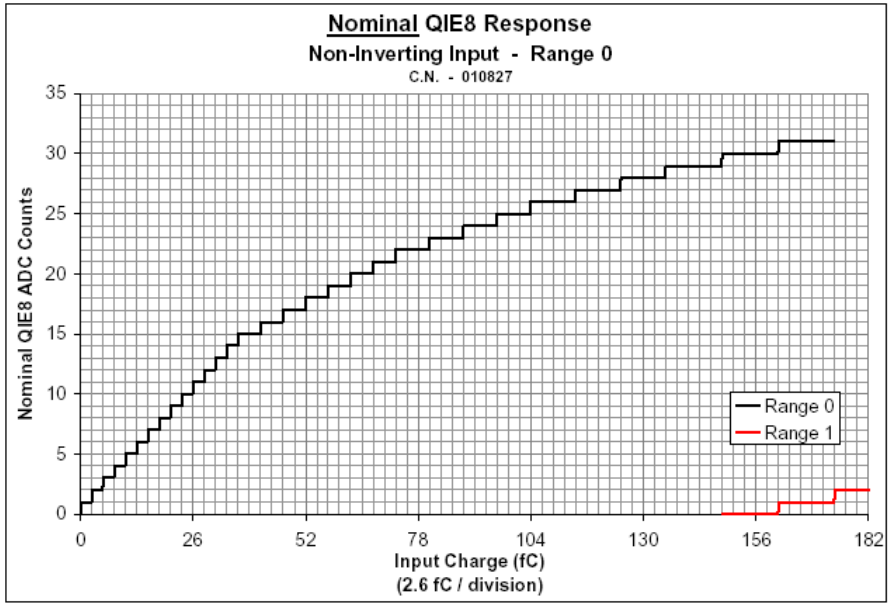
Goal is to submit production part by end of December '01

QIE under test

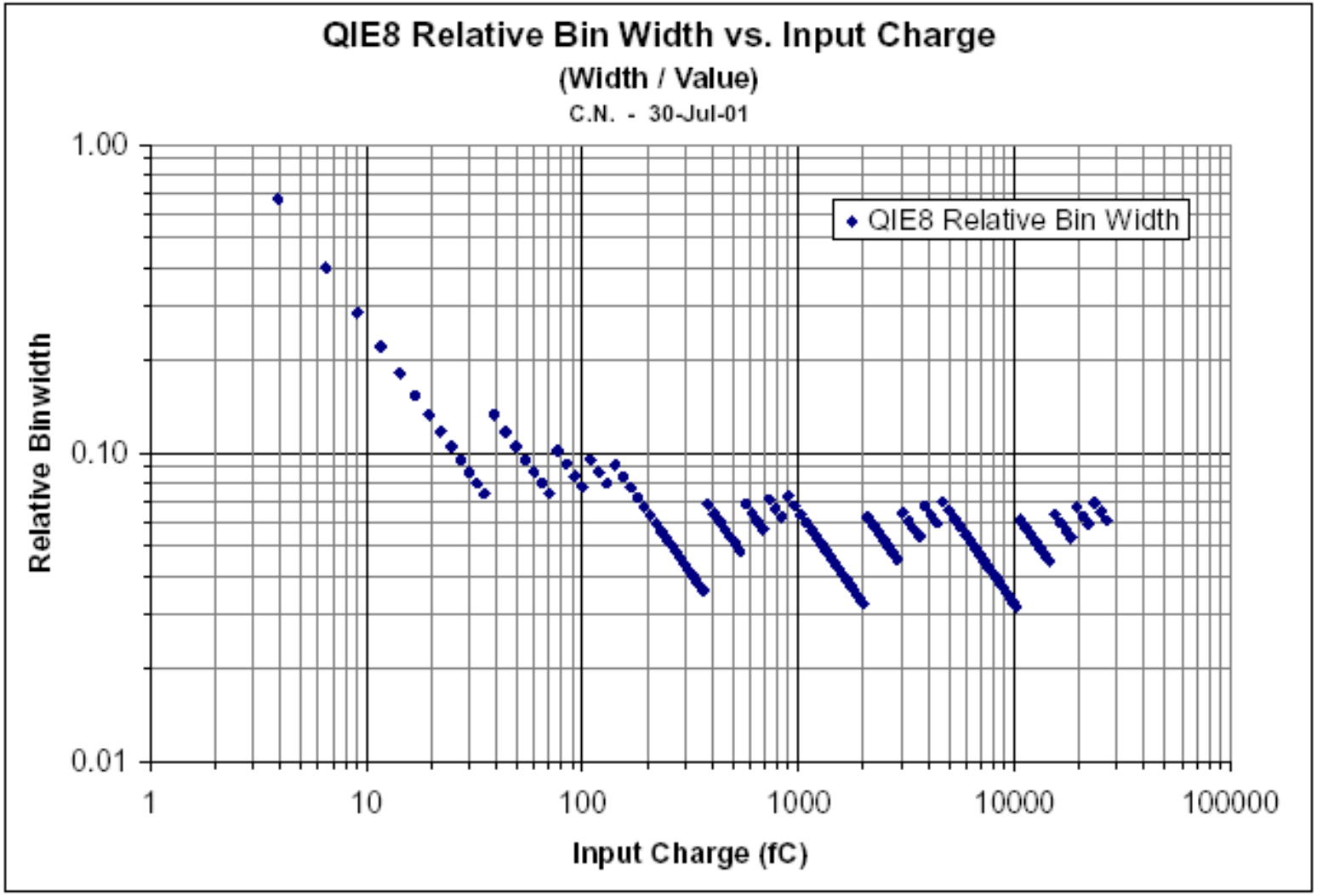


QIE Test Results





QIE Test Results



Channel Control ASIC

The CCA provides the following functions:

- The processing and synchronization of data from two QIEs,
- The provision of phase-adjusted QIE clocking signals to run the QIE charge integrator and Flash ADC,
- Checking of the accuracy of the Capacitor IDs, the Cap IDs from different QIEs should be in synchronization,
- The ability to force the QIE to use a given range,
- The ability to set Pedestal DAC values,
- The ability to issue a test pulse trigger,
- The provision of event synchronization checks – a crossing counter will be implemented and checked for accuracy with every beam turn marker,
- The ability to send a known pattern to the serial optic link,
- The ability to “reset” the QIE at a known and determined time,
- And, the ability to send and report on any detected errors at a known and determined time.

CCA Status

CCA submitted June 25, 2001

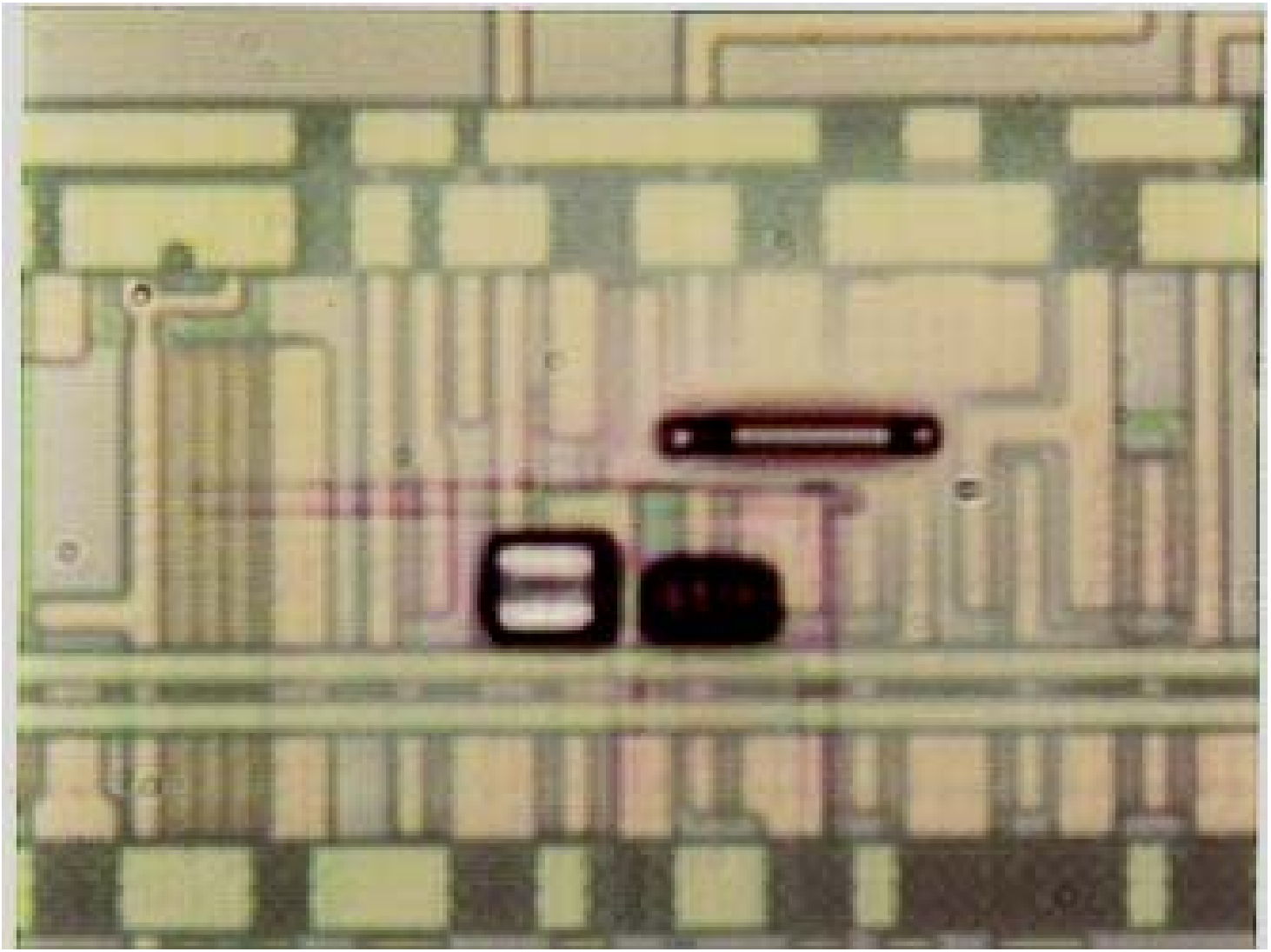
25 parts back Oct 11, 2001

Chips under test

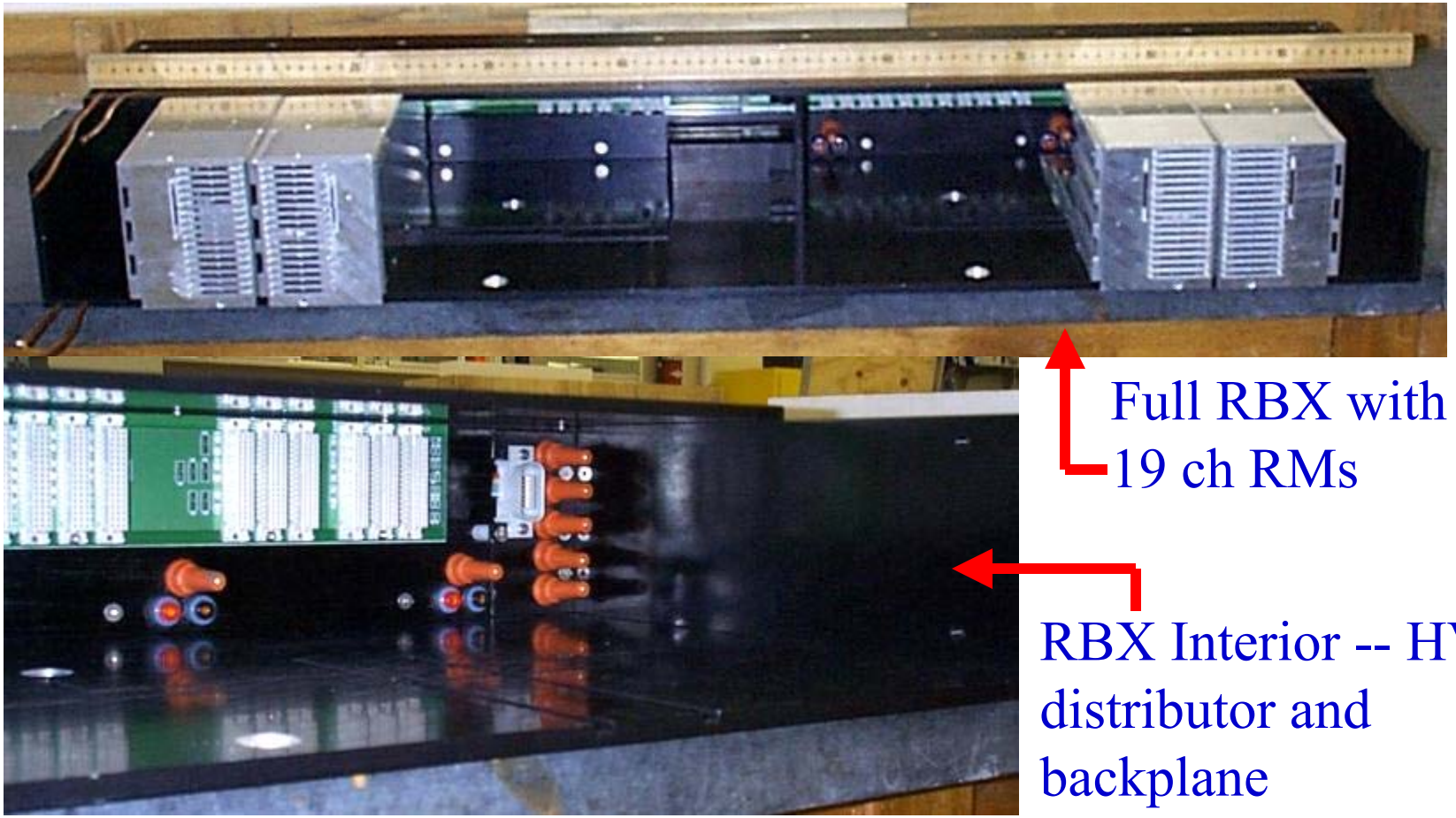
- **Problem with reads/writes to internal registers**
- **Problem with writes fixed with repair on chip (jumped out inverter)**
- **Problem with reads under study**
- **Other than reads, the CCA appears to be fully functional**

Goal is to submit production chip by year end

CCA ASIC Repair



HB RBX Assembly



Full RBX with 19 ch RMs

RBX Interior -- HV distributor and backplane

HB Backplane

Backplane

- ~87 CM LONG
- Provides Power
- Distributes 40 MHz Clock (3 load max)
- Provides path for RBXbus (serial communication bus)
- Temperature feedback

HB Backplane is ready for production

Bids are currently being taken

Backplanes will be back ~Feb '02

GOL Design Specifications

Synchronous (constant latency)

Transmission speed

- fast: 1.6 Gbps , 32 bit data input @ 40 MHz
- slow: 0.8 Gbps , 16 bit data input @ 40 MHz

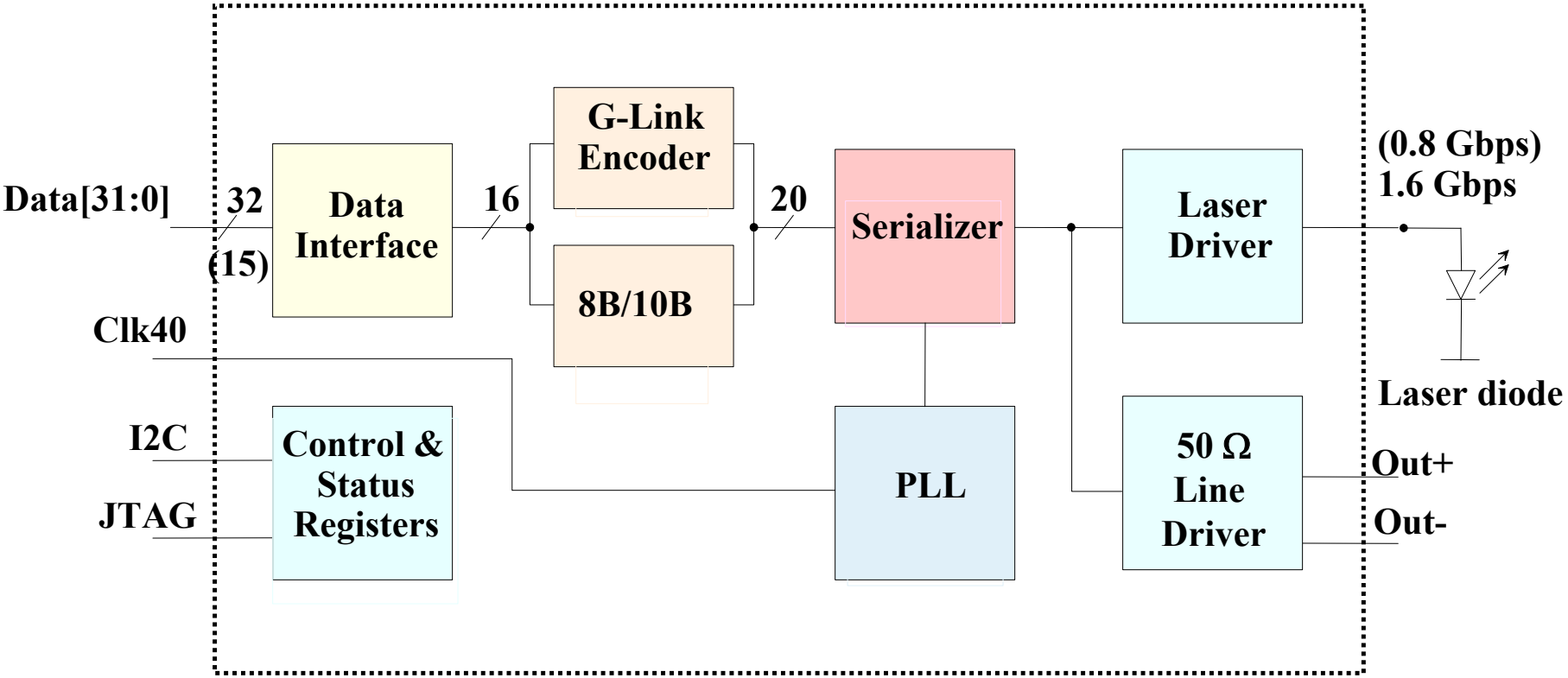
Two encoding schemes

- G-Link
- Fiber channel (8B/10B)

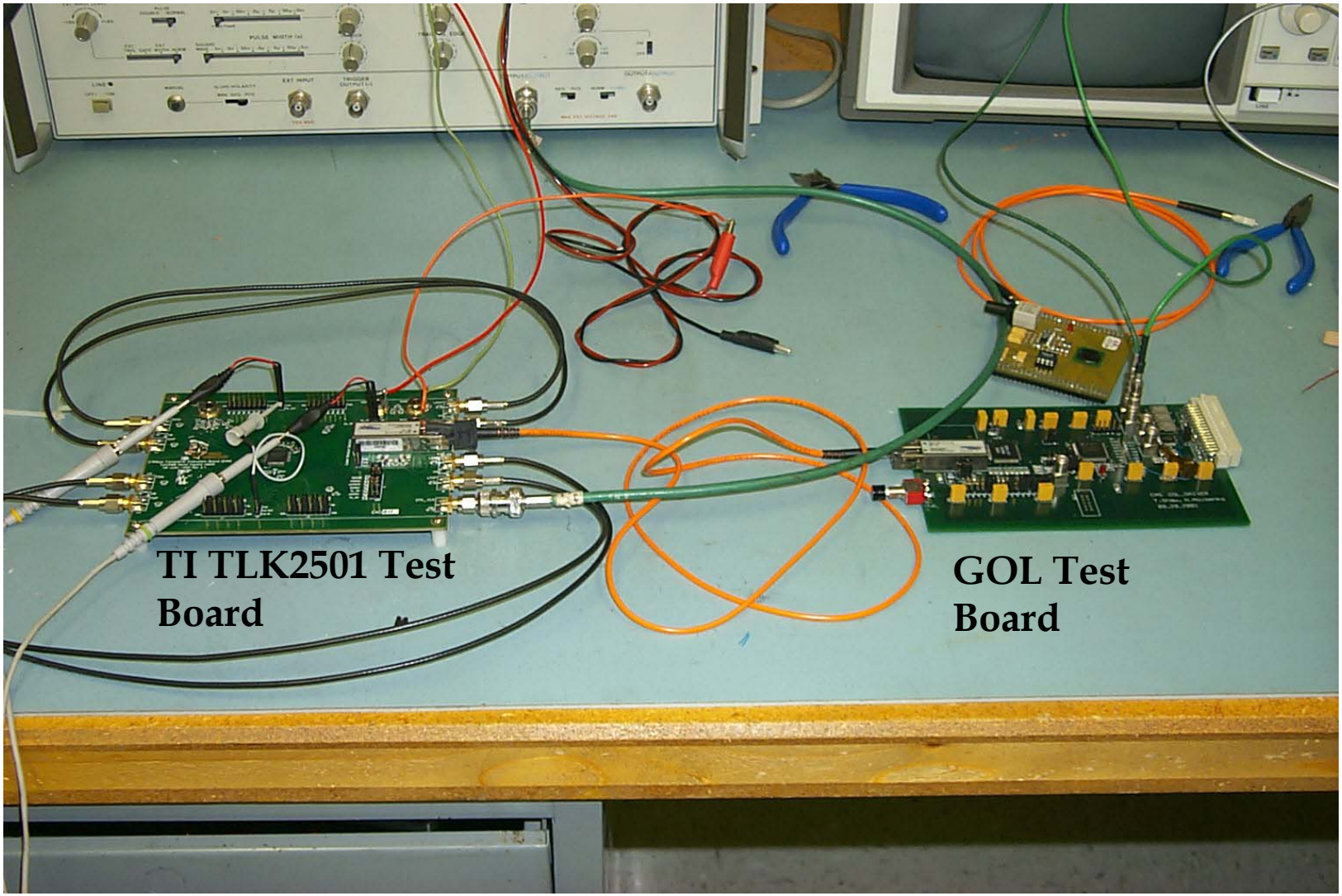
Interfaces for control and status registers

- I2C
- JTAG

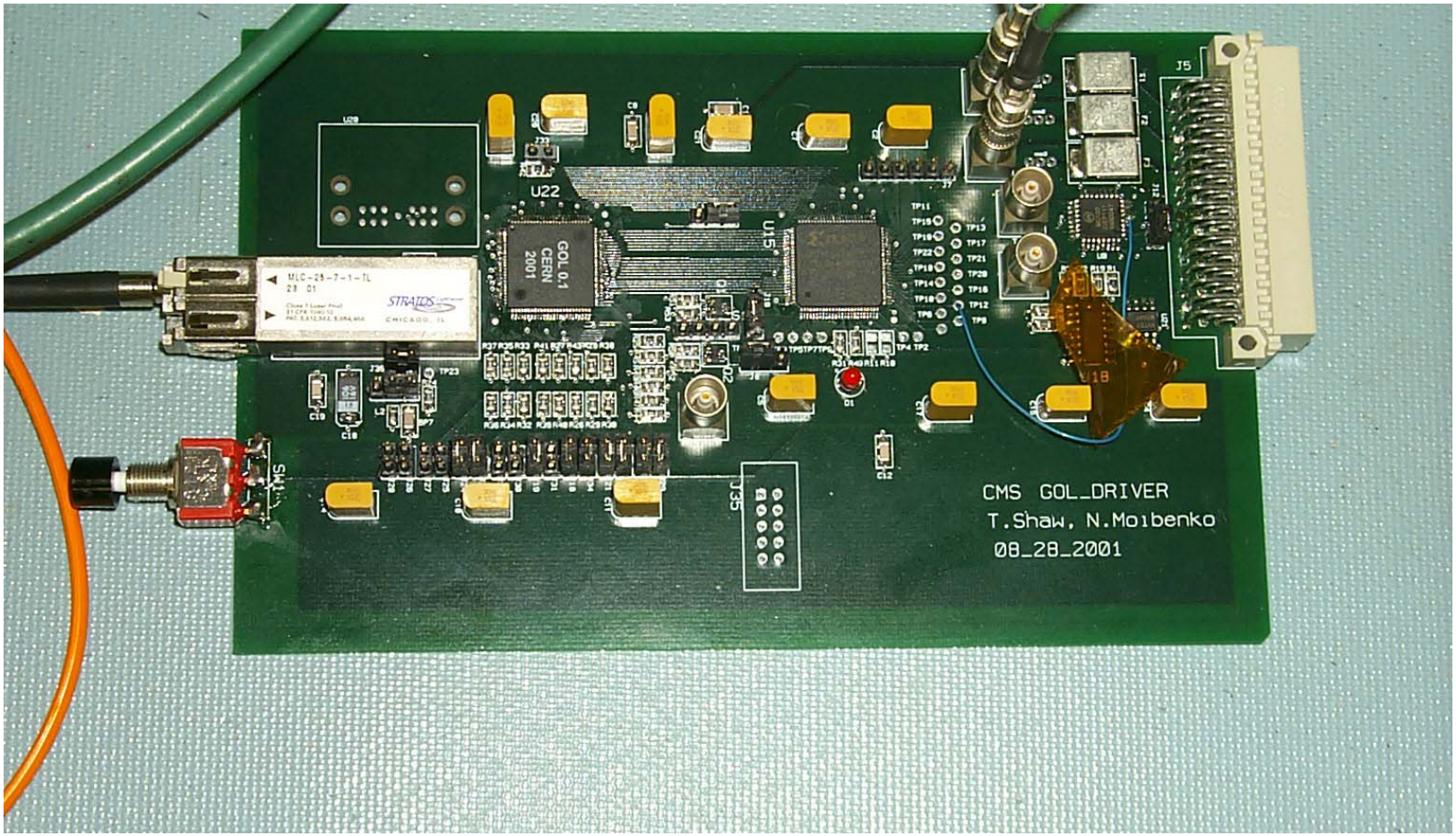
Gigabit link (G-Link, 8B/10B optional)



GOL Testing



GOL Test Board



GOL Test Results

GOL Configuration

- 32 bit mode
- 1.6 Gb/s
- Gigabit Ethernet Protocol

Data sent to TI TLK2501 Evaluation Board

- GOL clock is set to 45 MHz – this is a clock driven by fxn generator – not TTCrx (GOL known not to work with TTCrx clock at 1.6Gb/s)
- Data is alternating 0xAAAA AAAA and

  0x5555 5555
- The RX_ER (receive error) Flag on the Eval board is monitored
- No errors detected in 8+ hours of running

Optical Transmitter

HCAL is studying the use of a commercial VCSEL with custom packaging for use as an optical driver

- VCSEL operates at 850nm -> multimode fiber solution

The Tracker's solution of a Laser Transmitter is under study

- Laser Transmitter operates at 1300nm->allows single mode fiber operation

VCSEL Selection

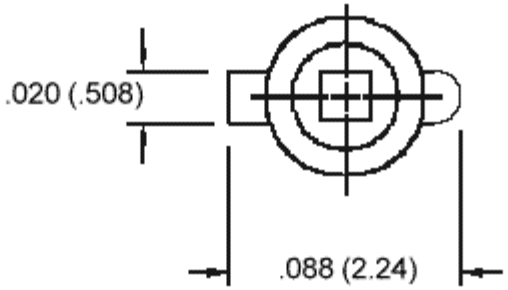
HFE4086-001

VCSEL Components, Data Communications, Flat Window Pillpack, Unattenuate optics, no back monitor photodiode

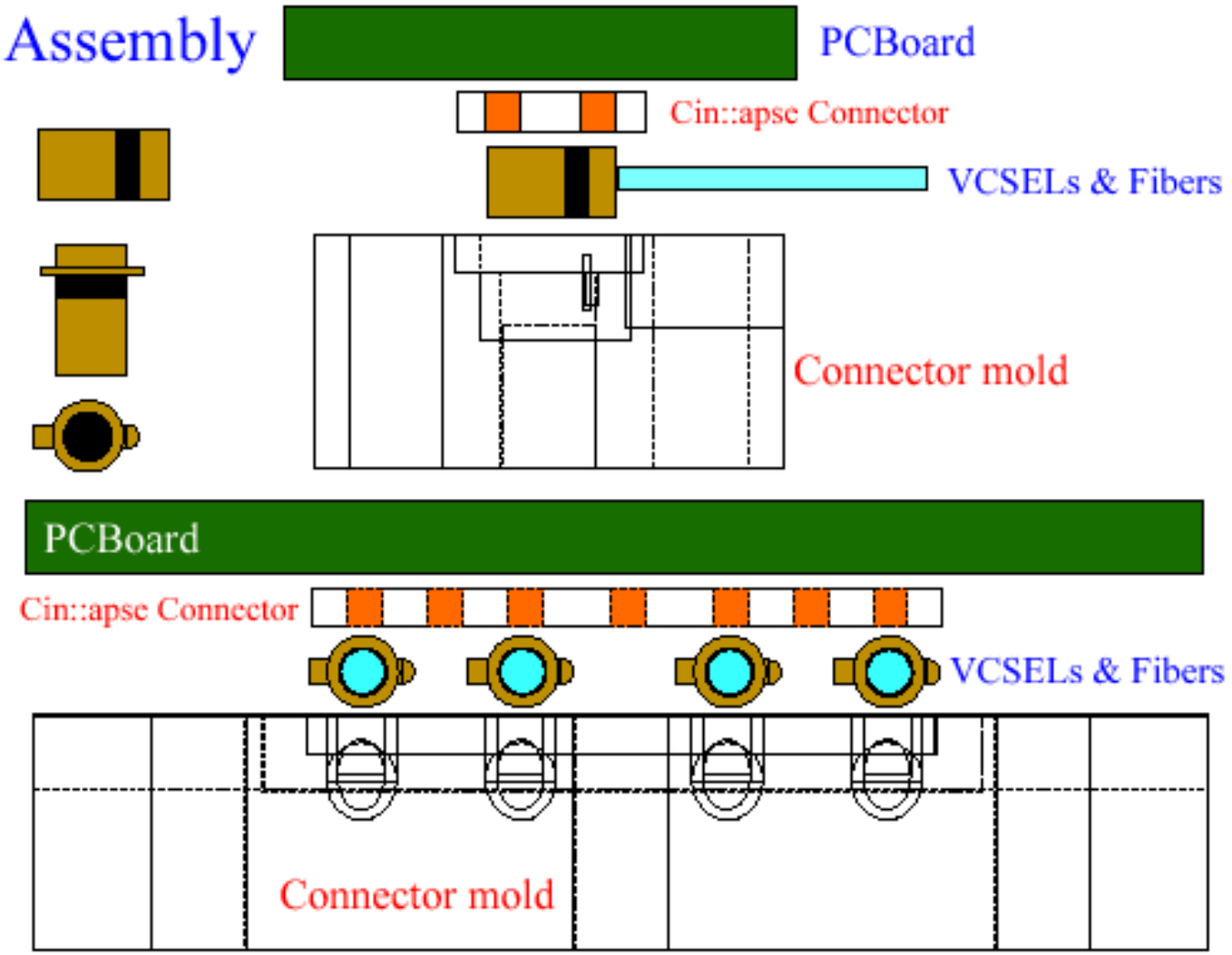
FEATURES

- Designed for drive currents between 5 mA and 15 mA
- Optimized for low dependence of electrical properties over temperature
- High speed > 1 Ghz
- Miniature flat-window, pill-pack package

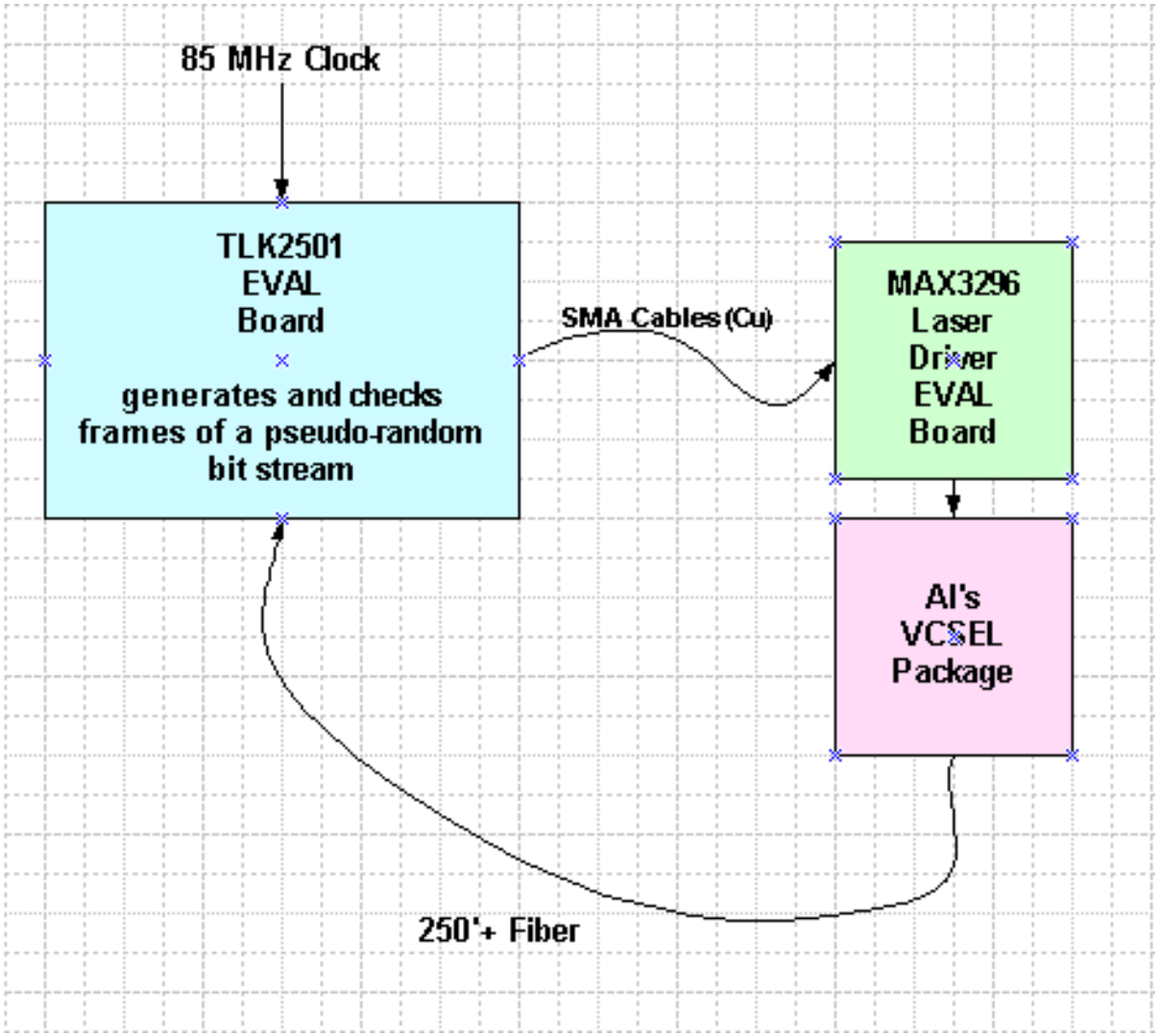
MOUNTING DIMENSIONS (for reference only): in./(mm)



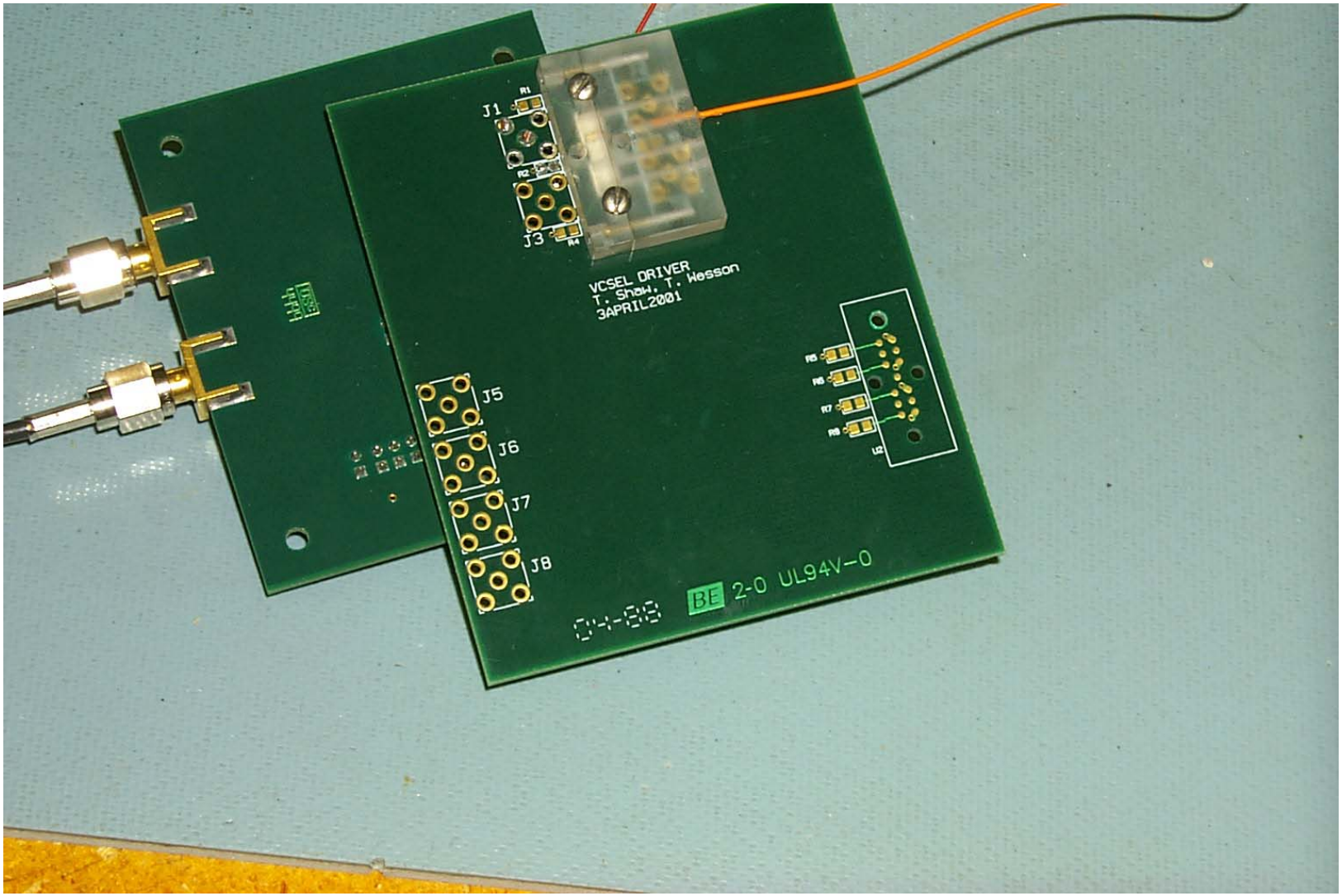
VCSEL Packaging



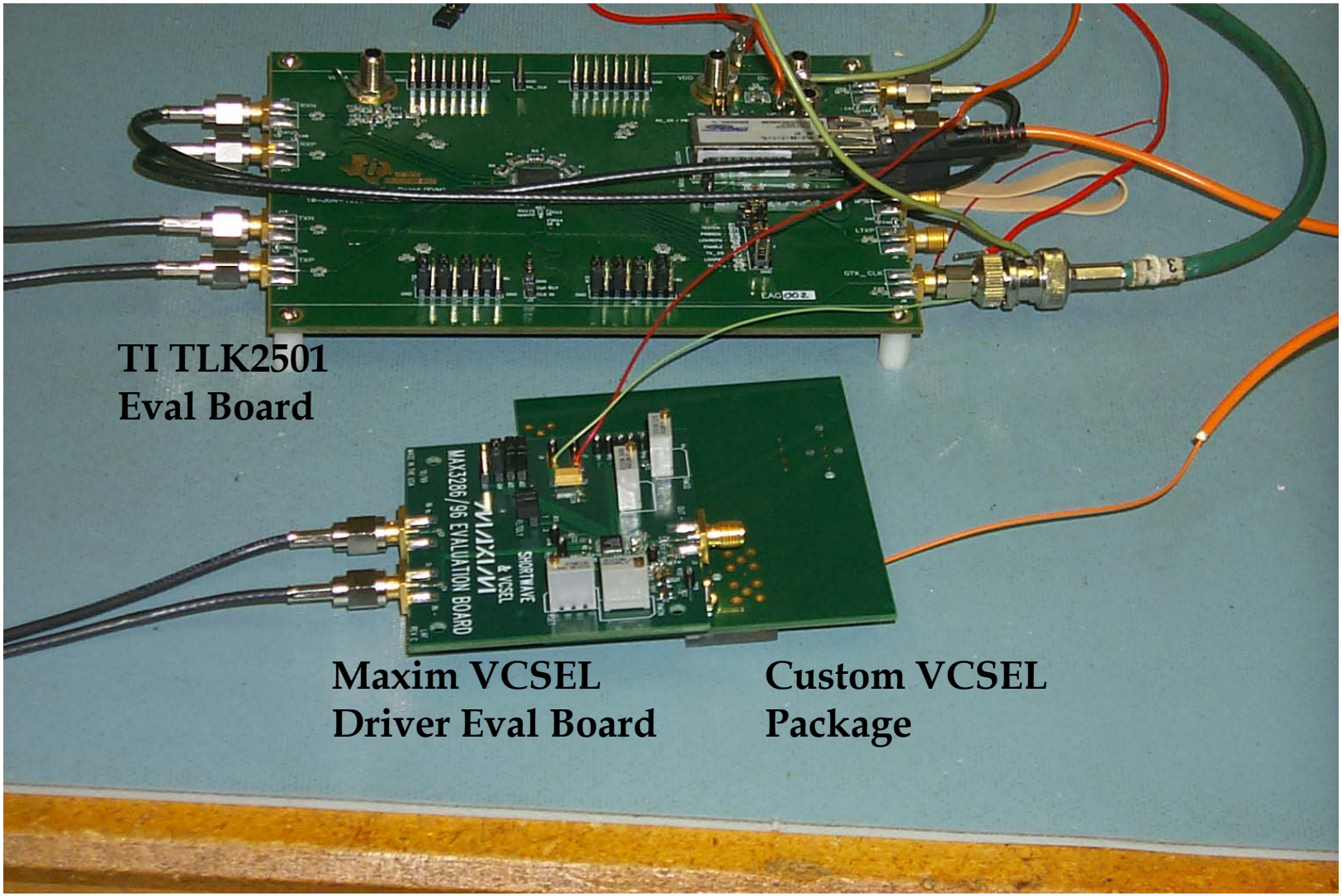
VCSEL Test Block Diagram



Prototype VCSEL Package



VCSEL Test


TI TLK2501
Eval Board
Maxim VCSEL
Driver Eval Board
Custom VCSEL
Package

VCSEL Test Results

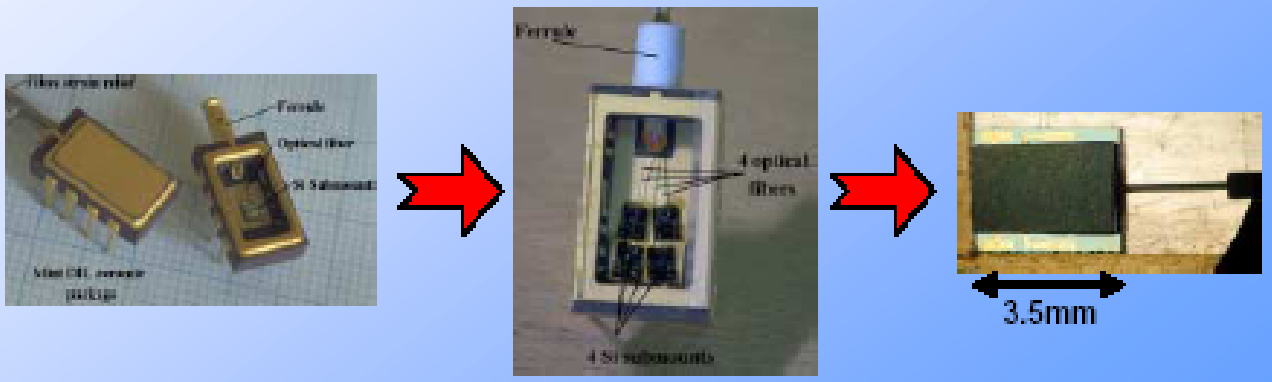
VCSEL Test Data Path

- Pseudorandom Data sent from TI TLK2501 Evaluation Board;
- Through Maxim VCSEL driver;
- Through custom VCSEL package;
- Through 250 feet of optic cable
- Back to TI TLK2501 Eval Board
- Serializer clock is set to 85 MHz
  - The RX_ER (receive error) Flag on the Eval board is monitored
  - No errors detected in 8+ hours of running

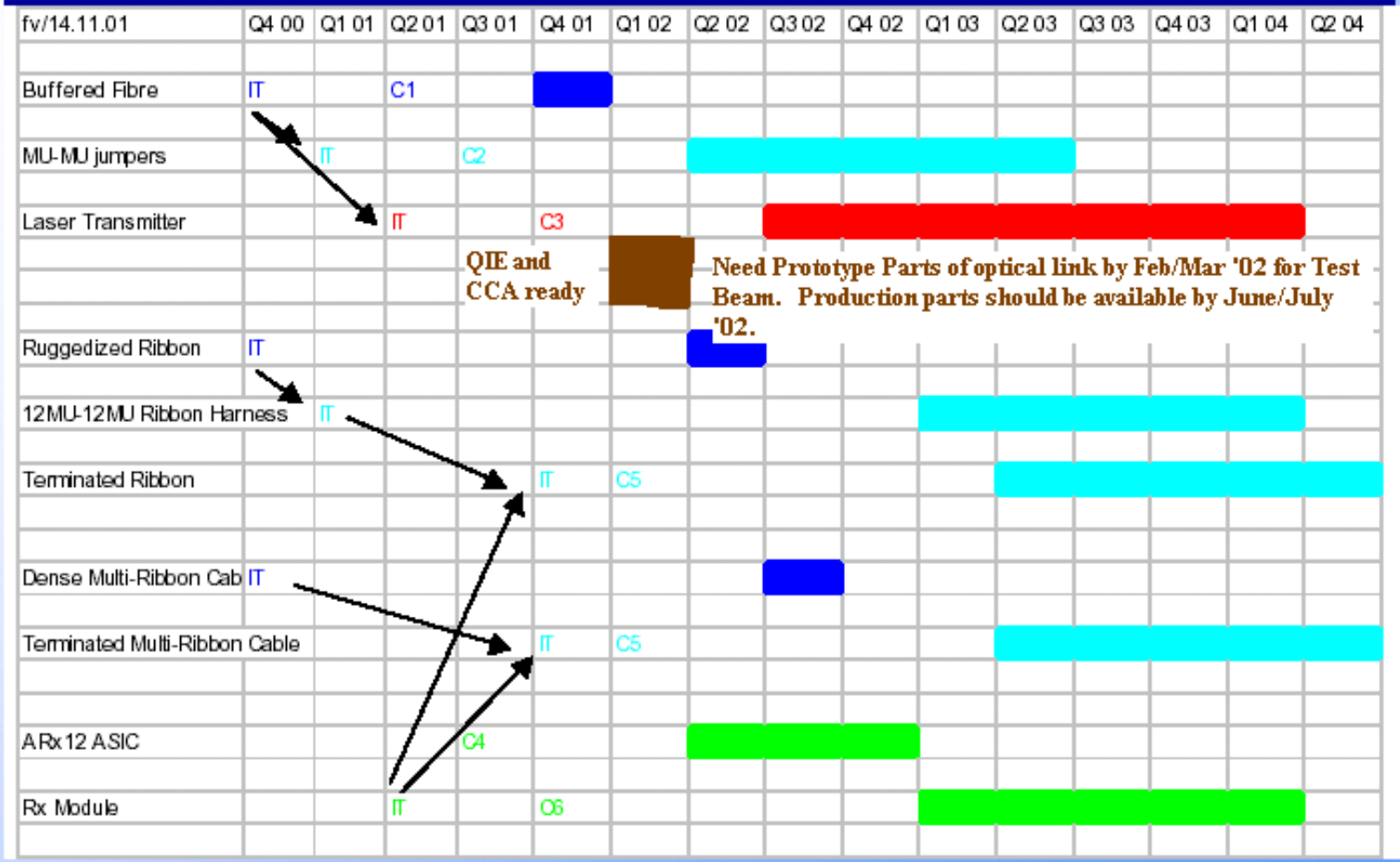
Tracker Laser Transmitter

Laser Transmitters

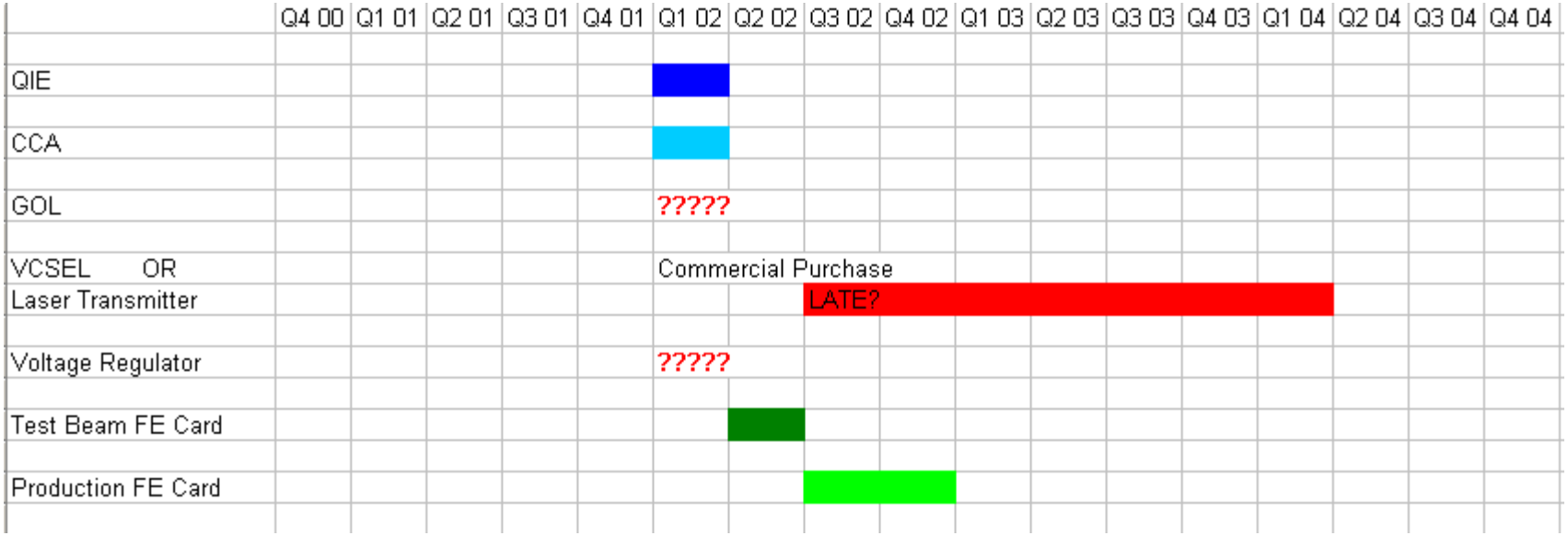
- **Evolution of devices**
  - Manufacturer contacts built up
    - Many manufacturers during project lifetime
    - Confident that most-suitable device chosen
    - Invitation to Tender complete – winner known (ST Microelectronics)
  - Final transmitter die commercially available (Mitsubishi COTS component)
  - Final transmitter package based upon commercial package
    - Very similar submount used in other packaging applications
  - Form factors & modularity now matched to Tracker application
    - Low mass, compact, non-magnetic



Production Schedule

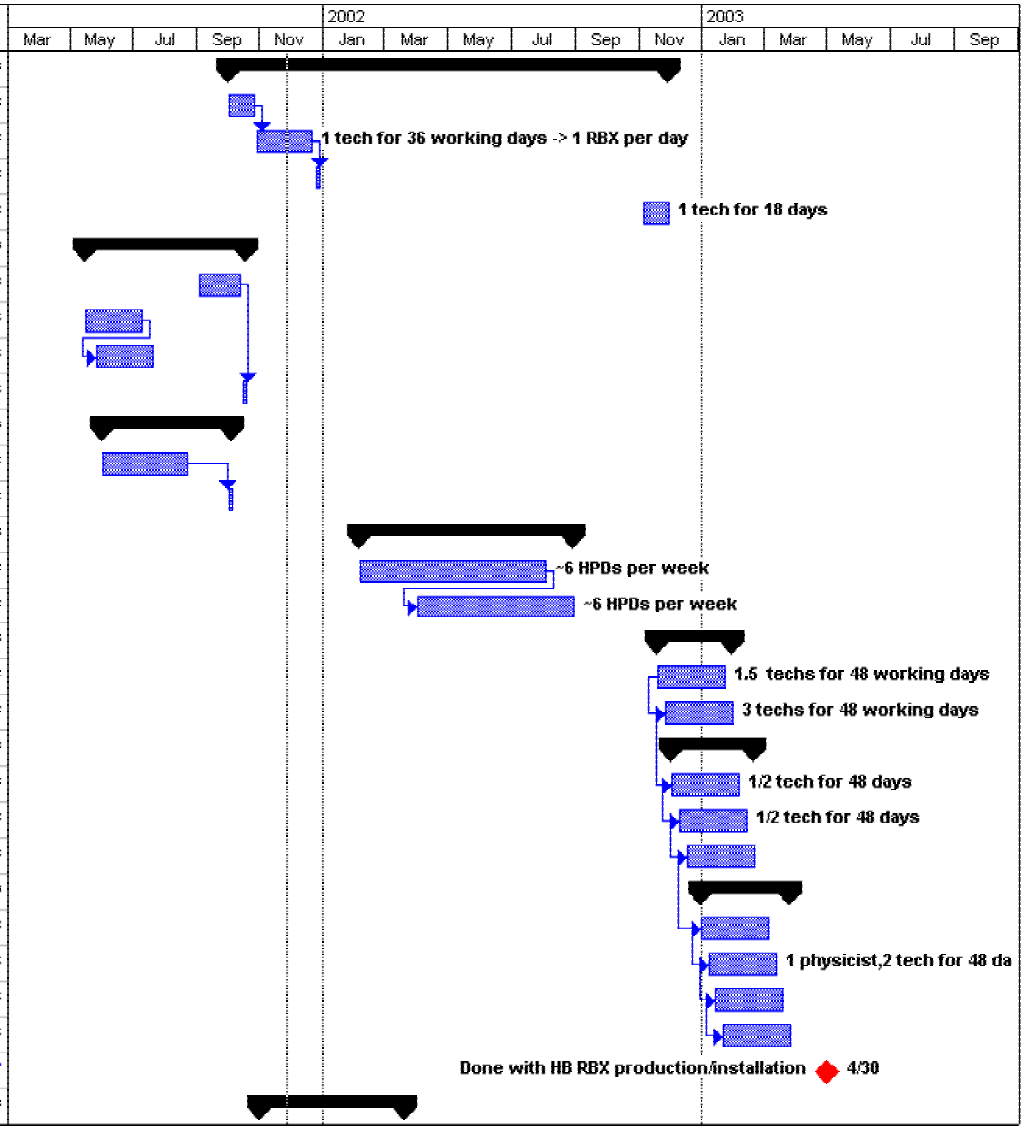


FE Module Production



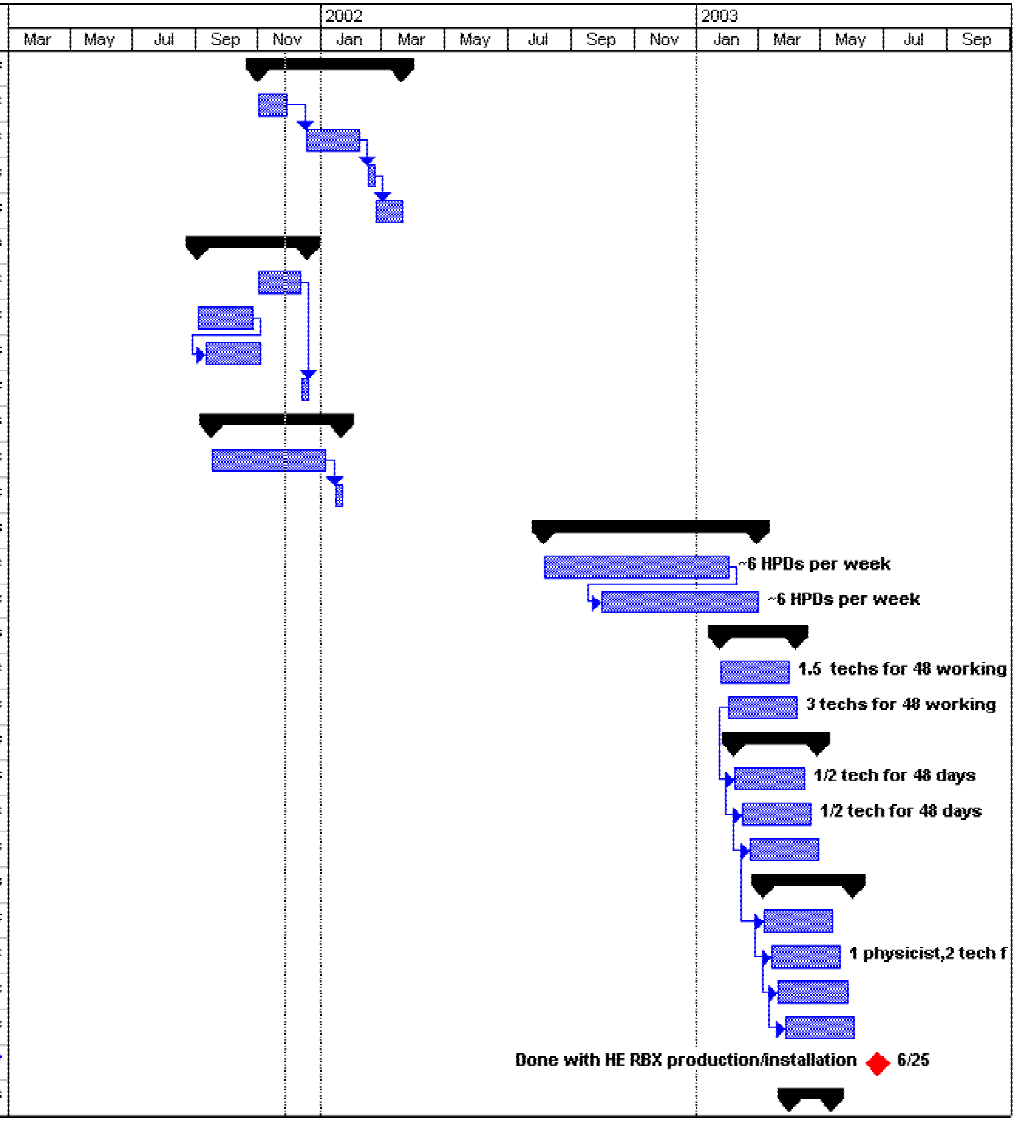
Production Schedule - HB

ID	Task Name	Start	Duration
2	**Produce 38 HB RBXs**	**Mon 10/1/01**	**305 days**
3	Manufacture HB Readout Boxes (RBX)	Mon 10/1/01	20 days
4	Assemble HB RBXs	Mon 10/29/01	40 days
5	Ship HB RBXs to FNAL	Mon 12/24/01	5 days
6	Install Backplanes in HB RBXs	Mon 11/4/02	20 days
7	**Manufacture 144 RM-19**	**Tue 5/15/01**	**114 days**
8	Manufacture 152 RM-19 parts	Mon 9/3/01	30 days
9	Manufacture 160 ODU-19 parts	Tue 5/15/01	40 days
10	Ship ODU-19 parts to Notre Dame	Fri 5/25/01	40 days
11	Ship RM-19 parts to Fermilab	Mon 10/15/01	5 days
12	**Assemble ODUs**	**Fri 6/1/01**	**91 days**
13	Assemble ODU-19	Fri 6/1/01	60 days
14	Ship ODU-19 to Fermilab	Mon 10/1/01	5 days
15	**Manufacture/Test HPDs**	**Mon 2/4/02**	**150 days**
16	Test Hybrid Photodetectors (HPDs)	Mon 2/4/02	130 days
17	Ship HPDs to Fermilab	Mon 4/1/02	110 days
18	**Readout Module Assembly**	**Mon 11/18/02**	**53 days**
19	Checkout Front end electronics modules(qty 432)	Mon 11/18/02	48 days
20	Assemble 144 RMs	Mon 11/25/02	48 days
21	**RBX Integration at FNAL**	**Mon 12/2/02**	**58 days**
22	Install/Checkout RMs in RBX	Mon 12/2/02	48 days
23	Burn-in RBXs	Mon 12/9/02	48 days
24	Ship RBXs to CERN	Mon 12/16/02	48 days
25	**RBX Integration at CERN**	**Mon 12/30/02**	**63 days**
26	Receive RBXs	Mon 12/30/02	48 days
27	Test RBXs	Mon 1/6/03	48 days
28	Install and Cable RBXs	Mon 1/13/03	48 days
29	Test Installed RBX	Mon 1/20/03	48 days
30	Milestone - done with HB by April 30 '03	Wed 4/30/03	1 day
31	**Produce 38 HE RBX**	**Thu 11/1/01**	**100 days**



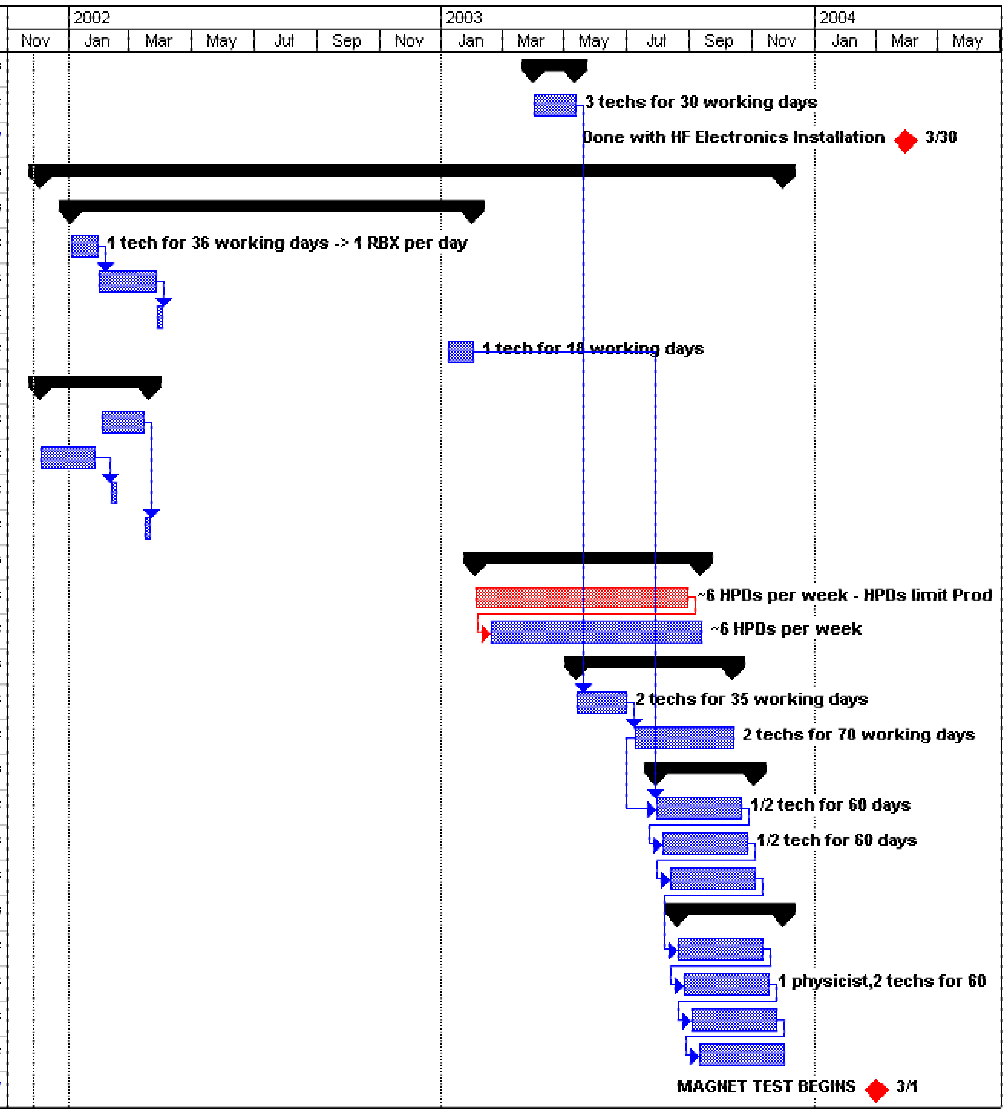
Production Schedule - HE

ID	Task Name	Start	Duration
31	**Produce 38 HE RBX**	**Thu 11/1/01**	**100 days**
32	MFR HE RBX	Thu 11/1/01	20 days
33	Assemble HE RBX	Mon 12/17/01	38 days
34	Ship HE RBX to Fermilab	Fri 2/15/02	5 days
35	Install Backplanes in HE RBX	Fri 2/22/02	19 days
36	**Manufacture 144 RM-19**	**Mon 9/3/01**	**78 days**
37	Manufacture 152 RM-19 parts	Thu 11/1/01	30 days
38	Manufacture 160 ODU-19 parts	Mon 9/3/01	40 days
39	Ship ODU-19 parts to Notre Dame	Mon 9/10/01	40 days
40	Ship RM-19 parts to Fermilab	Thu 12/13/01	5 days
41	**Assemble ODUs**	**Mon 9/17/01**	**91 days**
42	Assemble ODU-19	Mon 9/17/01	80 days
43	Ship ODU-19 to Fermilab	Tue 1/15/02	5 days
44	**Manufacture/Test HPDs**	**Mon 8/5/02**	**150 days**
45	Test Hybrid Photodetectors (HPDs)	Mon 8/5/02	130 days
46	Ship HPDs to Fermilab	Mon 9/30/02	110 days
47	**Readout Module Assembly**	**Thu 1/23/03**	**53 days**
48	Checkout Front end electronics modules(qty 432)	Thu 1/23/03	48 days
49	Assemble 144 RMs	Thu 1/30/03	48 days
50	**RBX Integration at FNAL**	**Thu 2/6/03**	**58 days**
51	Install/Checkout RMs in RBX	Thu 2/6/03	48 days
52	Burn-in RBXs	Thu 2/13/03	48 days
53	Ship RBXs to CERN	Thu 2/20/03	48 days
54	**RBX Integration at CERN**	**Thu 3/6/03**	**63 days**
55	Receive RBXs	Thu 3/6/03	48 days
56	Test RBXs	Thu 3/13/03	48 days
57	Install and Cable RBXs	Thu 3/20/03	48 days
58	Test Installed RBX	Thu 3/27/03	48 days
59	Milestone - done with HE by end of June 25 '03	Wed 6/25/03	1 day
60	**HF Electronics Production**	**Tue 4/1/03**	**30 days**



Production Schedule – HF/HO

ID	Task Name	Start	Duration
60	**HF Electronics Production**	**Tue 4/1/03**	**30 days**
61	Checkout Front end electronics modules (qty 413)	Tue 4/1/03	30 days
62	Milestone - done with HF by end of Mar 30 '04	Tue 3/30/04	1 day
63	**HO RBX Production/Installation**	**Mon 12/3/01**	**521 days**
64	**Produce 36 HO RBXs**	**Wed 1/2/02**	**283 days**
65	Manufacture HO Readout Boxes (RBX)	Wed 1/2/02	20 days
66	Assemble HO RBXs	Wed 1/30/02	40 days
67	Ship HO RBXs to FNAL	Wed 3/27/02	5 days
68	Install Backplanes in HO RBXs	Mon 1/6/03	20 days
69	**Produce 91 Readout Modules**	**Mon 12/3/01**	**79 days**
70	Manufacture 91 RM-19 Parts	Fri 2/1/02	30 days
71	Manufacture 154 ODU-19 parts	Mon 12/3/01	40 days
72	Ship ODU-19 parts to FNAL	Mon 2/11/02	5 days
73	Ship RM-19 parts to FNAL	Fri 3/15/02	5 days
74	**Manufacture/Test HPDs**	**Mon 2/3/03**	**160 days**
75	Test Hybrid Photodetectors (HPDs)	Mon 2/3/03	150 days
76	Ship HPDs to Fermilab	Mon 2/17/03	150 days
77	**Readout Module Assembly**	**Tue 5/13/03**	**110 days**
78	Checkout Front end electronics modules	Tue 5/13/03	35 days
79	Assemble 140 RMs	Tue 7/8/03	70 days
80	**RBX Integration at FNAL**	**Tue 7/29/03**	**70 days**
81	Install/Checkout RMs in RBX	Tue 7/29/03	60 days
82	Burn-in RBXs	Tue 8/5/03	60 days
83	Ship RBXs to CERN	Tue 8/12/03	60 days
84	**RBX Integration at CERN**	**Tue 8/19/03**	**75 days**
85	Receive RBXs	Tue 8/19/03	60 days
86	Test RBXs	Tue 8/26/03	60 days
87	Install and Cable RBXs	Tue 9/2/03	60 days
88	Test Installed RBX	Tue 9/9/03	60 days
89	GOAL is to be done with HO by end of Feb'04	Mon 3/1/04	1 day



FE – What's Next

Next 6 months

- Submit production CCA
- Submit production QIE
- Build ASIC chip testers
- Purchase GOL serializers
- Purchase rad hard Voltage Regulators (RD49)
- Choose VCSEL or "Tracker Laser Transmitter"
- Design 6 channel FE card for test beam
- Design 6 channel FE card for production
- Build card tester
- Prototype Clock and Control Module (CCM)